REMARKS

Present Status of the Application

The drawings are objected under 37 CFR 1.83(a). The Office Action rejected all presently-pending claims 1-2, 4-13. Specifically, the Office Action rejected claims 7 and 10-11 under 35 U.S.C. 102(a), as being anticipated by Bui (U.S. 6,163,049). The Office Action also rejected claims 13 under 35 U.S.C. 102(b) as being unpatentable over Gill. (U.S. 5,023,680). The Office Action rejected claims 1, 2, 4 and 5 under 35 U.S.C. 103(a), as obvious over Joo (U.S. 2001/0044187) in view of Bui (U.S. 6,163,049) and Park (U.S. 2001/0014510). The Office Action rejected claim 6 under 35 U.S.C. 103(a), as obvious over Joo (U.S. 2001/0044187) in view of Bui (U.S. 6,163,049), Park (U.S. 2001/0014510) and Choi (U.S. 6,340,827). The Office Action rejected claims 8-9 under 35 U.S.C. 103(a), as obvious over Bui (U.S. 6,163,049).

Applicants have added drawings and amended the specification to overcome the objection. Applicants have also canceled claims 2-3, 8-9 and 13, and amended claims 1, 7 to improve clarity. After entry of the foregoing amendments, claims 1, 4-7, 10-12 remain pending in the present application, and reconsideration of those claims is respectfully requested.

Discussion of objections

According to the OFFICE ACTION, the drawings were objected under 37 CFR 1.83(a) because the drawings do not show every feature of the invention specified in the claims. In

response thereto, applicants have added Fig. 3-5 and amended paragraph [0023] and [0024] for corresponding with the meaning of the sentence therein and no new matter is entered.

Discussion of Office Action Rejections

The Office Action rejected claims 7 and 10-11 under 35 U.S.C. 102(a), as being anticipated by Bui (U.S. 6,163,049). Applicants respectfully traverse the rejections for at least the reasons set forth below.

With respect to claim 7, independent claim 7 recites the features as follows:

7. A flash memory structure, comprising:
a tunneling oxide layer located upon a substrate;
a floating gate located upon the tunneling oxide layer;
a first oxide layer located upon the floating gate;
a high dielectric constant dielectric layer having a dielectric constant greater than 8 located upon the first oxide layer, wherein, together with the oxide layer, a dielectric stacked layer is formed, and a band gap value of the high dielectric constant dielectric layer is wide or wider than a band gap of silicon oxide;
a control gate formed on the high dielectric constant dielectric layer of the dielectric stacked layer; and
a source/drain region located within the substrate on the two sides of the floating gate.

Bui et al. disclosed a composite interpoly gate dielectric film 600 includes a LPCVD silicon dioxide layer 601, a silicon nitride layer 602 and a second oxide layer 603 comprising a material with a dielectric constant greater than that of silicon dioxide, e.g., greater than about 10. It is noted that Bui teaches the silicon oxide/silicon nitride/silicon oxide layer, with the **silicon nitride layer sandwiched between two oxide layers** as a composite film stack. However, claim 7 of the invention disclosed an inter-poly dielectric film comprising a first oxide layer and a high

dielectric constant dielectric layer, but not include a silicon nitride layer sandwiched between the two oxide layers. Besides, in claim 7 of the invention, the high dielectric constant dielectric layer has a band gap value ***wide or wider than*** a band gap of silicon oxide. Bui did not disclosed the issue about the band gap value, and did not teach about the high dielectric constant dielectric layer has a band gap value ***wide or wider than*** a band gap of silicon oxide.

Applicant respectfully submits that independent claim 7 patently define over the prior art references, and should be allowed. For at least the same reasons, dependent claims 10-12 patently define over the prior art as well.

The Office Action rejected claims 1, 2, 4 and 5 under 35 U.S.C. 103(a), as obvious over Joo (U.S. 2001/0044187) in view of Bui (U.S. 6,163,049) and Park (U.S. 2001/0014510). Applicants respectfully traverse the rejections for at least the reasons set forth below.

With respect to claim 1, independent claim 1 recites the features as follows:

1.A flash memory structure, comprising:
a tunneling oxide layer located upon a substrate;
a floating gate located upon the tunneling oxide layer;
a first oxide layer located upon the floating gate;
a high dielectric constant dielectric layer located upon the first oxide layer, wherein a dielectric constant of the high dielectric constant dielectric layer is greater than 8 and a band gap value of the high dielectric constant dielectric layer is less than a band gap value of silicon oxide;
a second oxide layer, located upon the high dielectric constant dielectric layer, wherein, together with the first oxide layer and the high dielectric constant dielectric layer, a dielectric stacked layer is formed;
a control gate formed on the second oxide layer of the dielectric stacked layer; and
a source/drain region located in the substrate on the two sides of the floating gate.

Joo et al. disclosed an inter-gate dielectric layer comprises a SiN film (or SiON film) 32, a TaON film 40 and a SiN film (or SiON film) 42, whrerin the TaON film 40 is a high dielectric constant dielectric layer. It is noted that Joo teaches the silicon nitride / high dielectric constant dielectric layer / silicon nitride layer (NHN), with the high dielectric constant dielectric layer sandwiched between two silicon nitride layers as a composite film stack. However, claim 1 of the invention disclosed an inter-gate dielectric film comprising a first oxide layer, a high dielectric constant dielectric layer and a second oxide layer, but not including a high dielectric constant dielectric layer sandwiched between two silicon nitride layers. Moreover, in claim 1 of the invention, the high dielectric constant dielectric layer has a band gap value less than a band gap of silicon oxide. Bui only teaches an inter-poly dielectric layer including a high dielectric constant dielectric layer (e.g., greater than about 10) and teaches away about the high dielectric constant dielectric layer should have a band gap value less than silicon oxide.

The Office Action considers it is obvious to modify the device of Joo to include the source/drain of Bui and the high dielectric constant dielectric layer of Park. If combined, Joo, Park and Bui do not achieve the claimed invention because Joo discloses the silicon nitride/ high dielectric constant dielectric layer /silicon nitride (NHN) layer between the floating gate and the control gate and Bui suggests the source/drain and Park suggests high dielectric constant dielectric layer has a dielectric constant greater than 25. Significantly, if you combine Joo, Park and Bui, a stacked NHN layer consisting of silicon nitride/ high dielectric constant dielectric layer /silicon nitride is obtained. Therefore, the combination of Joo, Park and Bui would dissuade one of ordinary skill in the art from arriving at the present invention.

In determining whether even a prima facie showing of obviousness exists, it is necessary to ascertain whether the prior art teachings suggest the claimed combination to one of ordinary skill in the art. The burden of establishing a prima facie showing of obviousness rests upon the Patent Office, and that burden has not been met. The only suggestion to combine the various features from each patent comes from the applicant's specification and claims.

For at least the foregoing reasons, Applicant respectfully submits that independent claims 1 patently define over the prior art references, and should be allowed. For at least the same reasons, dependent claims 4-6 patently define over the prior art as well.

Application No.: 09/990,397 **Docket No.: JCLA7289**

CONCLUSION

For at least the foregoing reasons, it is believed that the pending claims 1, 4-7, 10-12 are in proper condition for allowance. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

Respectfully submitted,
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Date: 12/23/2003

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